WHAT IS CLAIMED IS:

1. A method for fabricating a transistor having a fully silicided gate, comprising:

providing a substrate with a semi-finished transistor formed thereon, wherein the semi-finished transistor comprises a gate dielectric film, a silicon gate on the gate dielectric film, a cap layer on the silicon gate, a spacer on sidewalls of the silicon gate and a source/drain region in the substrate beside the silicon gate;

forming a raised source/drain on the source/drain region;

removing the cap layer; and

performing a full silicidation process to fully silicide the silicon gate.

2. The method of claim 1, wherein the raised source/drain is formed with a selective epitaxial growth (SEG) process, and a silicide contact is also formed from the raised source/drain in the full silicidation process.

3. The method of claim 1, wherein the full silicidation process comprises:

forming a metal layer over the substrate;

performing a first annealing step to induce a reaction between the silicon gate and the metal layer, such that the silicon gate is fully silicided; and

removing the remaining metal layer.

4. The method of claim 3, wherein the metal layer comprises a nickel layer.

5. The method of claim 3, wherein the metal layer comprises a cobalt layer.

6. The method of claim 3, wherein the full silicidation step further comprises performing a second annealing step after the remaining metal layer is removed.

7. The method of claim 1, wherein the gate dielectric film comprises a silicon oxide film or a silicon oxide/silicon nitride (ON) composite film.

8. The method of claim 1, wherein the silicon gate comprises a polysilicon gate.

9. The method of claim 1, wherein the cap layer comprises an anti-reflection layer.

10. The method of claim 9, wherein the anti-reflection layer comprises silicon nitride or silicon oxynitride.

11. The method of claim 1, wherein the source/drain region includes a source/drain extension under the spacer.

12. A method for fabricating a transistor having a fully silicided gate, comprising:

sequentially forming a gate dielectric film, a silicon layer and an anti-reflection layer on a silicon substrate;

patterning the anti-reflection layer, the silicon layer and the gate dielectric film to form a gate structure, wherein the silicon layer is patterned into a silicon gate;

forming a source/drain extension in the substrate beside the gate structure;

forming a spacer on sidewalls of the gate structure;

forming a source/drain region in the substrate beside the spacer;

performing a selective epitaxial growth (SEG) process to form a raised source/drain on the source/drain region;

removing the anti-reflection layer; and

performing a full silicidation process to fully silicide the silicon gate and simultaneously to form a silicide contact from the raised source/drain.

13. The method of claim 12, wherein the full silicidation process comprises:

forming a metal layer over the substrate covering the silicon gate and the raised source/drain;

performing a first annealing step to induce a reaction between the silicon gate, the raised source/drain react and the metal layer, such that the silicon gate is fully silicided; and

removing the remaining metal layer.

14. The method of claim 13, wherein the metal layer comprises a nickel layer.

15. The method of claim 13, wherein the metal layer comprises a cobalt layer.

16. The method of claim 13, wherein the full silicidation process further comprises performing a second annealing step after the remaining metal layer is removed.

17. The method of claim 12, wherein the gate dielectric film comprises a silicon oxide film or a silicon oxide/silicon nitride (ON) composite film.

18. The method of claim 12, wherein the silicon layer comprises a polysilicon layer.

19. The method of claim 12, wherein the anti-reflection layer comprises silicon nitride.

20. The method of claim 12, wherein the anti-reflection layer comprises silicon oxynitride.